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6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/832,466	GRIFFIN ET AL.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The body of this **rejection** can be found in paper no. 4.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-10, 12-14, and 16-22 are rejected under 35 U.S.C. 102(a) as being anticipated by US 6141769 to Petivan et al. Referring to claim 1, Petivan et al. disclose a fault-tolerant server comprising: (a) a communications link (From figure 3, 38.); (b) a first computing element in electrical communication with the communications link, the first computing element providing a first output to the communications link (From figure 3, 46A. Further, from the abstract, "wherein the first system module further includes a first control device which coordinates transfer of first transaction information between the first processor bus and each of the first I/O bus or the second I/O bus or the third I/O bus"); (c) a second

computing element in electrical communication with the communications link, the second computing element providing a second output to the communications link (From figure 3, 46B. Further, from the abstract, "wherein the second system module further includes a second control device which coordinates transfer of second transaction information between the second processor bus and each of the first I/O bus or the second I/O bus or the third I/O bus".); (d) a first local input-output (I/O) subsystem in electrical communication with the first computing element and the communications link (From the abstract, "wherein the first system module further includes a first control device which coordinates transfer of first transaction information between the first processor bus and each of the first I/O bus or the second I/O bus or the third I/O bus"); and (e) a second local I/O subsystem in electrical communication with the second computing element and the communications link (From the abstract, "wherein the second system module further includes a second control device which coordinates transfer of second transaction information between the second processor bus and each of the first I/O bus or the second I/O bus or the third I/O bus"), wherein at least one of the first local I/O subsystem and the second local I/O subsystem compares the first output and the second output and indicates a fault of at least one of the first computing element and the second computing element upon the detection of a miscompare of the first output and the second output (From the abstract, "wherein the first system module includes first comparison logic which compares first transaction information with corresponding second transaction information". Further, from line 25 of column 4, "If any of the comparisons indicate that the

information transacted by any module in the course of a given bus transaction differs from the information transacted by a neighboring module, then the bridge logic detecting the mismatch signals a fault to all three processors."), and wherein the first local I/O subsystem is in electrical communication with the second local I/O subsystem via a synch bus to synchronize the first local I/O subsystem and the second local I/O subsystem (From line 60 of column 4, "For example, in order to read data from an I/O device during normal synchronous system operation, all three processors synchronously direct a read request to the I/O controller local to the module that controls the target I/O device. The subject I/O controller responds by reading the requested information from the target I/O device via the bus local to the one particular module. The bridge logic unit and the backplane interconnects cooperate to send the read information to the other two modules." Further, from line 7 of column 5, "Conversely, in order to write data to an I/O device during normal synchronous system operation, all three processors synchronously direct a write request to the I/O controller local to the module that controls the target I/O device. The information to be written is actually provided to the I/O controller interface by the processor local to the target I/O device. Thus, although all three processors provide to their respective local buses the same write information, only the processor local to the target I/O device presents the information to the I/O controller interface. The subject I/O controller responds by causing the write information to be written to the target I/O device. In the course of the write operation, the bridge logic unit and the backplane interconnects cooperate to send the write information provided by

each processor to the bridge logic units of the neighboring modules." Further, from line 39 of column 5, "Each module's reference clock signal is broadcast over the backplane, via lines 38', to the other modules." Further, with emphasis, from line 47 of column 6, "In addition to starting in the same state, all processors should receive the same inputs. This calls for several synchronizing actions. For example, external interrupts should be synchronized and presented to all processors at the same time. This is accomplished by the bridge logic unit as explained in detail below. DMA requests also should be synchronized. The bridge logic units also accomplish this synchronization, along with other DMA overhead. Processor reads from I/O devices should be stable and deterministic. In order to ensure stability and determinism, relevant signals such as SBus "acknowledge", for instance, are synchronized in the bridge logic units.").

Referring to claim 2, Petivan et al. disclose each computing element further comprises a respective Central Processing Unit (CPU) and a respective local mass storage device (From line 19 of column 14, "The basic architecture of the present invention provides three independent SCSI channels-one on each system module. Several levels of fault tolerance can be implemented depending on application requirements.").

Referring to claim 3, Petivan et al. disclose the communications link further comprises a respective switching fabric in electrical communication with the CPU and at least one of the first local I/O subsystem and the second local I/O subsystem (From line 45 of column 2, "The system module 46 is coupled to an interconnect unit 38 which interconnects the three system modules, and which

interconnects actual I/O connectors (not shown) to the three system modules. In a presently preferred embodiment, the interconnect unit 38 is implemented as a PC board and may be referred to as a "backplane." The interconnect unit 38 includes first connections 40 whereby the respective bridge logic unit 52 of each module can broadcast the module's "own" I/O bus transaction information for delivery to other modules. The interconnect 38 unit also includes second connections 42 whereby the respective bridge logic unit of each module can receive bus transaction information broadcast by the bridge logic unit of neighboring "upstream" and "downstream" modules. The present interconnect unit also has disposed on it the physical I/O connectors (details not shown) which communicate with the I/O controllers on the system modules." Further, from line 19 of column 22, "Thus, in the current embodiment, during a processor write operation, the switch 96 on the target module is closed directly connecting the processor bus and the I/O bus." Further, from line 14 of column 23, "A backplane (BP) multiplexer 80 receives digital information from upstream and downstream modules; selects between information from an upstream module and information from a downstream module; and provides the selected information to the backplane/own data multiplexer 82 and to the up/own address multiplexer 84. An up/down selection control signal UDISEL (1) controls the BP multiplexer 80 selection of upstream or downstream information.").

Referring to claims 4 and 16, Petivan et al. disclose a priority module to assign a priority to each respective computing element (From line 18 of column 12, "The strategy employed by the diagnostic procedure of the current

embodiment involves analyzing patterns of miscompares. A single miscompare may not necessarily signify an error. Thus, multiple miscompares are evaluated in order to discern a pattern which may suggest which module(s) are suspect. The suspect modules are then "scored", in a manner described below, in order to determine which of the suspect modules is likely to be faulty." Further, from line 6 of column 13, "In general, when a module is suspected but not replaced it becomes a more likely candidate for replacement the next time or times it is suspected. The above approach aims to resolve another diagnostic ambiguity. In general, when operating with only two modules (such as after the failure of a third module) it is often impossible to identify the faulty module after a miscompare. However, if one of the remaining modules has been a suspect in the past, it can be regarded as the more likely offender in the two-module case.").

Referring to claims 5 and 17, Petivan et al. disclose each local I/O subsystem further comprises I/O fault-tolerant logic to determine whether at least one of the first computing element and the second computing element is faulty based on the priority (From line 23 of column 12, "The suspect modules are then "scored", in a manner described below, in order to determine which of the suspect modules is likely to be faulty.").

Referring to claims 6 and 18, Petivan et al. disclose each local I/O subsystem further comprises I/O fault-tolerant logic to determine whether the first output and the second output are comparatively equivalent (From line 65 of column 3, "The bridge logic unit of each module compares the information transacted by that module with information transacted by a neighboring module."

Further, from line 8 of column 4, "Note that different information may be compared for different transactions since different control and data are presented during different transactions.").

Referring to claim 7, Petivan et al. disclose each I/O fault-tolerant logic comprises a comparator (From line 65 of column 3, "The bridge logic unit of each module compares the information transacted by that module with information transacted by a neighboring module." Further, see figure 6.).

Referring to claim 8, Petivan et al. disclose each I/O fault-tolerant logic further comprises a buffer to hold at least one of the first output and the second output from at least one of the CPUs (From line 18 of column 9, "Thus, an error detected by any enabled module is reported to the respective control/status logic 74 of the other modules. The control/status logic on each module instructs its transaction latch 70 to "freeze" (retain) transaction information for the transaction for which an error has been detected. Connections, described more fully below, between each module's local I/O bus 56 and its local transaction latch 70 and its local control/status logic 74 allow the local processor (not shown) to examine the contents of the transaction latch 70 and the results of the faulty comparison for diagnostic purposes." Further, from line 50 of column 21, "The transaction latches (only the latch 70 of one module shown) temporarily store the transaction information so that it can be provided to corresponding processors for diagnostic analysis in the event that the pair-wise comparison process detects a possible error." Further, from line 67 of column 23, "A transaction data error storage 70-1 receives input from the own data storage 83. This latch stores the data

information when there is a miscompare (i.e., error). The address error transaction storage 70-2 receives input from the own address storage 88. This latch stores address information when there is a miscompare. A control error storage 70-3 receives input from the processor bus control lines. This latch stores control information when there is a incomparable.").

Referring to claim 9, Petivan et al. disclose a voter delay buffer to store at least one of the first instruction and the second instruction upon a miscompare of the first output and the second output (From line 18 of column 9, "Thus, an error detected by any enabled module is reported to the respective control/status logic 74 of the other modules. The control/status logic on each module instructs its transaction latch 70 to "freeze" (retain) transaction information for the transaction for which an error has been detected. Connections, described more fully below, between each module's local I/O bus 56 and its local transaction latch 70 and its local control/status logic 74 allow the local processor (not shown) to examine the contents of the transaction latch 70 and the results of the faulty comparison for diagnostic purposes." Further, from line 50 of column 21, "The transaction latches (only the latch 70 of one module shown) temporarily store the transaction information so that it can be provided to corresponding processors for diagnostic analysis in the event that the pair-wise comparison process detects a possible error." Further, from line 67 of column 23, "A transaction data error storage 70-1 receives input from the own data storage 83. This latch stores the data information when there is a miscompare (i.e., error). The address error transaction storage 70-2 receives input from the own address storage 88. This

latch stores address information when there is a miscompare. A control error storage 70-3 receives input from the processor bus control lines. This latch stores control information when there is a incomparable.").

Referring to claim 10, Petivan et al. disclose a delay module in electrical communication with one of the first and second local I/O subsystems to delay transmission of at least one output to one of the first and second local I/O subsystems (From line 59 of column 23, "In contrast, the own data storage unit 83 is part of the bridge pipeline. It holds data before it goes into the data compare 72-1.").

Referring to claim 12, Petivan et al. disclose each respective local I/O subsystem is located on a same motherboard as the respective computing element (From line 36 of column 2, "The presently preferred embodiment includes three redundant system modules, each of which essentially implements a SPARCstation 5 computer system. In addition to the SS5 implementation, each system board includes a bridge logic unit that allows the three system boards to exchange data, compare signals in order to detect faults, share I/O devices, and connect to a common backplane. Referring to the illustrative drawing of FIG. 2, there is shown a generalized block diagram of a system module 46 in accordance with a current implementation of the invention. The system module 46 includes a processor 48 and system memory 50. The module 46 also includes Input/Output (I/O) controllers 54 and a bridge logic unit 52. The processor 48 and bridge logic unit 52 are connected via a bus 56, in this case an SBus. The I/O controllers 54 and bridge logic unit 52 are connected via a bus

57, in this case an SBus." Further, from line 61 of column 2, "It will be appreciated, of course, that the physical location of the I/O connectors and the I/O controllers may be changed without departing from the scope of the invention.").

Referring to claims 13 and 22, Petivan et al. disclose (a) establishing communication between the first computing element and a communications link (From figure 3, 38.); (b) establishing communication between the second computing element and the communications link (From figure 3, 38); (c) transmitting, by the first computing element, a first output to the communications link (From the abstract, "wherein the first system module further includes a first control device which coordinates transfer of first transaction information between the first processor bus and each of the first I/O bus or the second I/O bus or the third I/O bus"); (d) transmitting, by the second computing element, a second output to the communications link (From the abstract, "wherein the second system module further includes a second control device which coordinates transfer of second transaction information between the second processor bus and each of the first I/O bus or the second I/O bus or the third I/O bus".); and (e) comparing, by at least one of a local input-output (I/O) subsystem of the first computing element and a local I/O subsystem of the second computing element, the first output and the second output and indicating a fault of at least one of the first computing element and the second computing element in response thereto (From the abstract, "wherein the first system module includes first comparison logic which compares first transaction information with corresponding second

transaction information". Further, from line 25 of column 4, "If any of the comparisons indicate that the information transacted by any module in the course of a given bus transaction differs from the information transacted by a neighboring module, then the bridge logic detecting the mismatch signals a fault to all three processors."), wherein the local I/O subsystem of the first computing element is in electrical communication with the local I/O subsystem of the second computing element via a sync bus to enable synchronization of the local I/O subsystems (From line 60 of column 4, "For example, in order to read data from an I/O device during normal synchronous system operation, all three processors synchronously direct a read request to the I/O controller local to the module that controls the target I/O device. The subject I/O controller responds by reading the requested information from the target I/O device via the bus local to the one particular module. The bridge logic unit and the backplane interconnects cooperate to send the read information to the other two modules." Further, from line 7 of column 5, "Conversely, in order to write data to an I/O device during normal synchronous system operation, all three processors synchronously direct a write request to the I/O controller local to the module that controls the target I/O device. The information to be written is actually provided to the I/O controller interface by the processor local to the target I/O device. Thus, although all three processors provide to their respective local buses the same write information, only the processor local to the target I/O device presents the information to the I/O controller interface. The subject I/O controller responds by causing the write information to be written to the target I/O device. In the course of the write

operation, the bridge logic unit and the backplane interconnects cooperate to send the write information provided by each processor to the bridge logic units of the neighboring modules." Further, from line 39 of column 5, "Each module's reference clock signal is broadcast over the backplane, via lines 38', to the other modules." Further, with emphasis, from line 47 of column 6, "In addition to starting in the same state, all processors should receive the same inputs. This calls for several synchronizing actions. For example, external interrupts should be synchronized and presented to all processors at the same time. This is accomplished by the bridge logic unit as explained in detail below. DMA requests also should be synchronized. The bridge logic units also accomplish this synchronization, along with other DMA overhead. Processor reads from I/O devices should be stable and deterministic. In order to ensure stability and determinism, relevant signals such as SBus "acknowledge", for instance, are synchronized in the bridge logic units.").

Referring to claim 14, Petivan et al. disclose the step of transmitting a stop command to each computing element when the first instruction does not equal the second instruction (From line 18 of column 9, "Thus, an error detected by any enabled module is reported to the respective control/status logic 74 of the other modules. The control/status logic on each module instructs its transaction latch 70 to "freeze" retain) transaction information for the transaction for which an error has been detected.").

Referring to claim 19, Petivan et al. disclose storing at least one of the first output and the second output from at least one of the computing elements for a

predetermined amount of time (From line 18 of column 9, "Thus, an error detected by any enabled module is reported to the respective control/status logic 74 of the other modules. The control/status logic on each module instructs its transaction latch 70 to "freeze" (retain) transaction information for the transaction for which an error has been detected. Connections, described more fully below, between each module's local I/O bus 56 and its local transaction latch 70 and its local control/status logic 74 allow the local processor (not shown) to examine the contents of the transaction latch 70 and the results of the faulty comparison for diagnostic purposes." Further, from line 50 of column 21, "The transaction latches (only the latch 70 of one module shown) temporarily store the transaction information so that it can be provided to corresponding processors for diagnostic analysis in the event that the pair-wise comparison process detects a possible error." Further, from line 67 of column 23, "A transaction data error storage 70-1 receives input from the own data storage 83. This latch stores the data information when there is a miscompare (i.e., error). The address error transaction storage 70-2 receives input from the own address storage 88. This latch stores address information when there is a miscompare. A control error storage 70-3 receives input from the processor bus control lines. This latch stores control information when there is a incomparable.").

Referring to claim 20, Petivan et al. disclose storing at least one of the first output and the second output upon a miscompare of the first output and the second output (From line 18 of column 9, "Thus, an error detected by any enabled module is reported to the respective control/status logic 74 of the other

modules. The control/status logic on each module instructs its transaction latch 70 to "freeze" (retain) transaction information for the transaction for which an error has been detected. Connections, described more fully below, between each module's local I/O bus 56 and its local transaction latch 70 and its local control/status logic 74 allow the local processor (not shown) to examine the contents of the transaction latch 70 and the results of the faulty comparison for diagnostic purposes." Further, from line 50 of column 21, "The transaction latches (only the latch 70 of one module shown) temporarily store the transaction information so that it can be provided to corresponding processors for diagnostic analysis in the event that the pair-wise comparison process detects a possible error." Further, from line 67 of column 23, "A transaction data error storage 70-1 receives input from the own data storage 83. This latch stores the data information when there is a miscompare (i.e., error). The address error transaction storage 70-2 receives input from the own address storage 88. This latch stores address information when there is a miscompare. A control error storage 70-3 receives input from the processor bus control lines. This latch stores control information when there is a incomparable.").

Referring to claim 21, Petivan et al. disclose the transmitting of the first output and the transmitting of the second output to the communications link occur simultaneously (From line 61 of column 3, "During normal operation, the processors and the processor memory on the three modules operate in clock synchronization. That is, the same operations always are transacted simultaneously on the three processor buses during normal operation. The

bridge logic unit of each module compares the information transacted by that module with information transacted by a neighboring module." Further, from line 65 of column 7, "As the Read/Write transaction progresses, each bridge logic unit sends the relevant bus signals (address, data, and control) over the backplane to its downstream neighbor. Simultaneously, each receives the corresponding information from its upstream neighbor, and compares its own local transaction information to that sent by its upstream neighbor.").

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6141769 to Petivan et al. as applied to claims 1 and 13 above. Referring to claim 11, although Petivan et al. do not specifically disclose the first computing element and the second computing element further comprise a 1U rack-mount motherboard, rack-mounting equipment is notoriously well known in the art. Examiner takes official notice for a 1U rack-mount form factor circuitry, such circuitry comprising a motherboard. A person of ordinary skill in the art at the time of the invention would have been motivated to use a 1U rack-mount form factor because he or she did not want to simply put the equipment on a shelf, it provides a more manageable footprint, it looks professional and industrial, and

because it is a matter of design.

Referring to claim 15, although Petivan et al. do not specifically disclose detecting an error introduced by the communications link, detecting errors from a communication link is notoriously well known in the art. Examiner takes official notice for error detection and correction in communications, examples of which are CRC, ECC, and parity. A person of ordinary skill in the art at the time of the invention would have been motivated to ensure correct data was transferred because incorrect data worsens data processing.

Response to Arguments

6. Applicant's arguments filed 14 May 2004 have been fully considered but they are not persuasive. Regarding Applicant's argument that one of ordinary skill in the art would understand the meaning of the word "instruction" when reading the word in the various contexts in combination with the teaching of the Specification taken as a whole, there is no question that it *may* be understood, as Examiner has shown that it can be understood. However, the issue at hand is that the specification as written is unclear and unnecessarily obfuscated. Furthermore, Examiner has shown that it can become unclear as to what point the "instruction" is compared for a miscompare. Further regarding Applicant's statement that Examiner suggests a CPU's proper processing of instructions is identified by comparing instructions prior to their execution by CPU boards, this is the very misunderstanding that Examiner wishes to avoid. It is suggested that Applicant amend to avoid any further confusion.

Regarding Applicant's argument that Petivan et al. does not disclose synchronization of first and second local I/O subsystems via a sync bus, Applicant does not disclose the extent, nature, or duration of any such synchronization. While Petivan et al. has disclosed that their I/O controllers are not synchronized, Petivan et al. goes further to say that such asynchronicity is defined by the fact that "different operations may be initiated during the same time interval on the three I/O buses". Further, Examiner has shown where Petivan et al. is synchronous given the loose limiting language amended to by Applicant.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is

(703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

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